1. The total number of bytes required to store both Euclid's algorithm and relPrime as well as any memory variables or constants.

**Euclid: 200B**

**relPrime: 614B**

2. The total number instructions executed when relPrime is called with 0x13B0 (the result should be 0x000B using the algorithm specified in the project specifications).

**Total Instructions: 36630 instructions**

3. The total number of cycles required to execute `relPrime under the same conditions as Step 2.

**Total Cycles: 4009 cycles**

4. The average cycles per instruction based on the data collected in Steps 2 and 3.

**Average Cycles: 1.09 cycles**

5. The cycle time for your design (from the Xilinx Synthesis report – look for the Timing summary).

**\_\_ ns =\_\_ Mhz**

6. The total execution time for relPrime under the same conditions as Step 2.

**Total Execution Time: 7,355,580ns**

7. The gate count for your entire design (from the Xilinx Map report). This appears to have changed/is omitted in recent version. Extra credit for any group that finds a reasonable way to estimate the equivalent gate count from the data in the Xilinx reports.

**Gate Count:**

8. The device utilization summary (from the Xilinx Synthesis report).

**Device Utilization Report**